EE 505

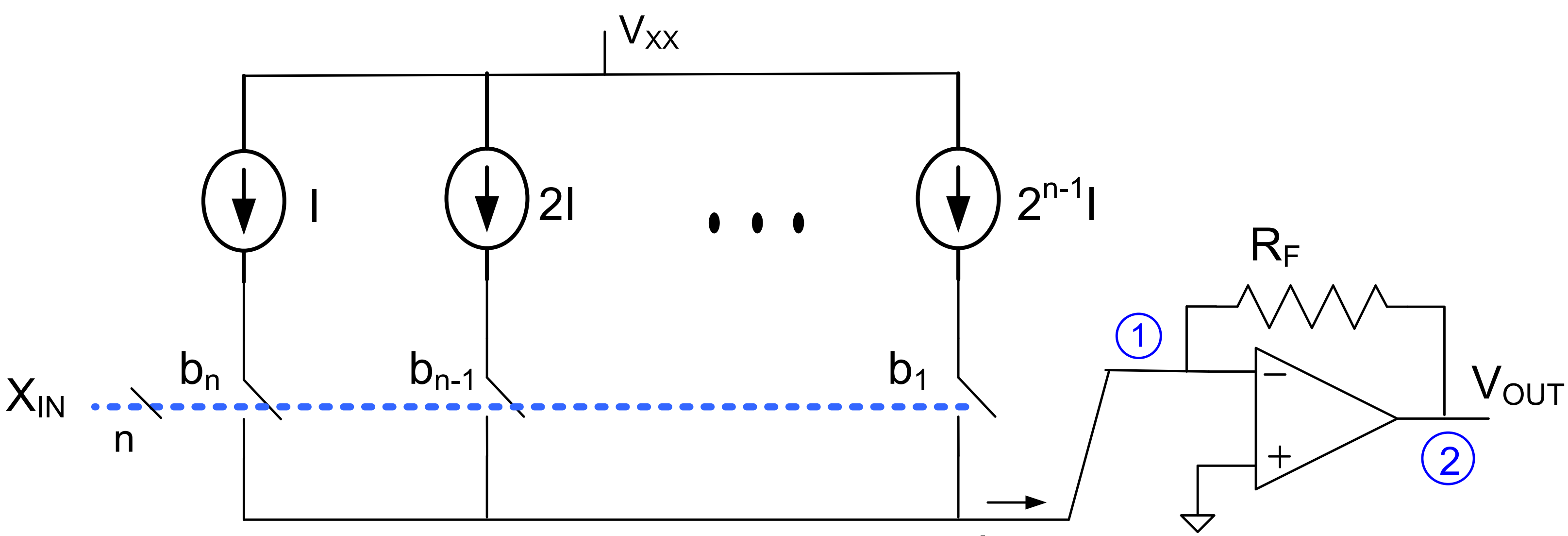
Lecture 18

Dynamic Current Source Matching

Charge Redistribution DACs

Review from Last Lecture

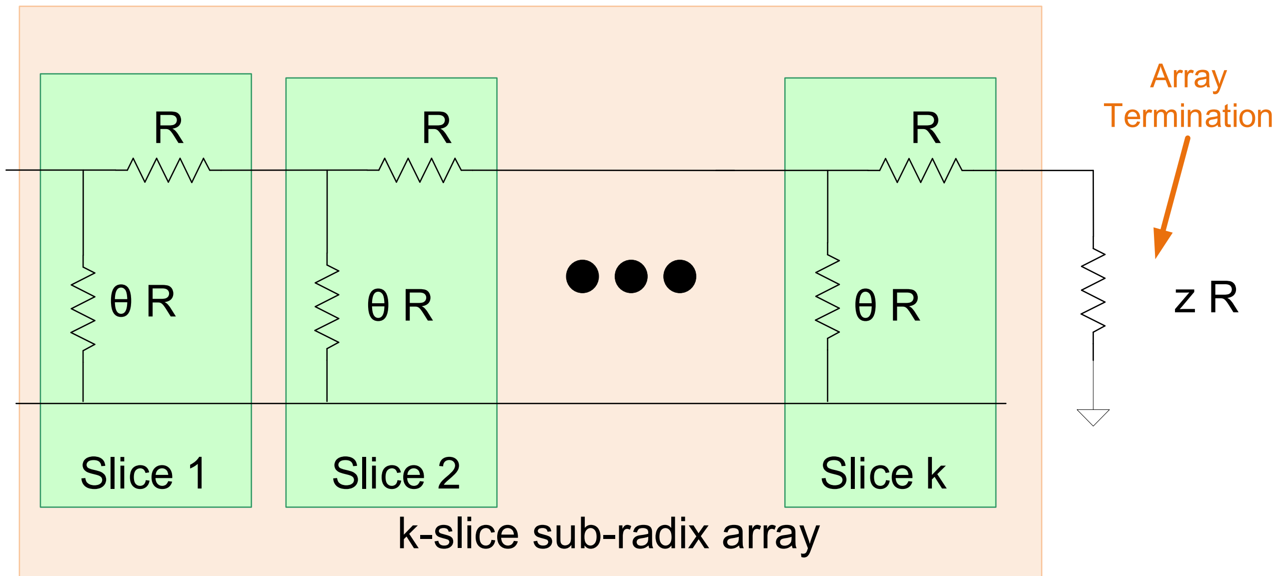
Current Steering DAC



$I_{OUT} = kI$

Review from Last Lecture

Sub-radix Array



Typically $2.1 < \theta < 2.5$

Termination resistor must be selected so that same attenuation is maintained

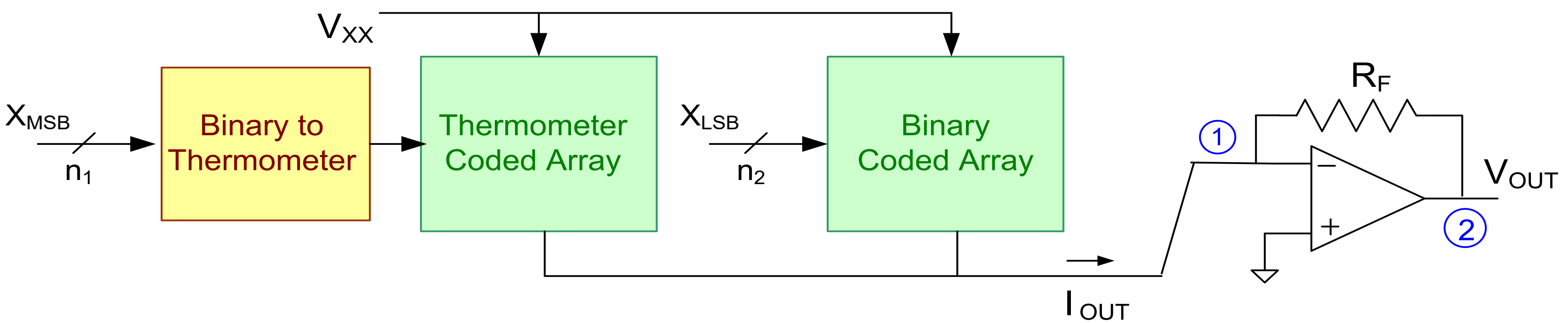
Often only the first n_1 MSB "slices" will be sub-radix

Effective number of bits when using sub-radix array will be less than k

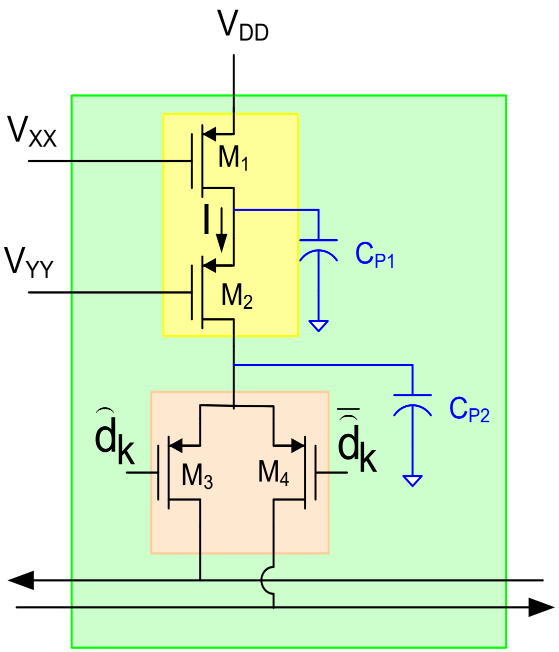
Can be calibrated to obtain very low DNL (and maybe INL) with small area

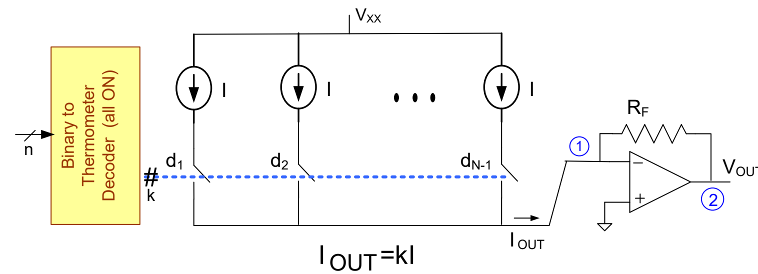
Review from Last Lecture

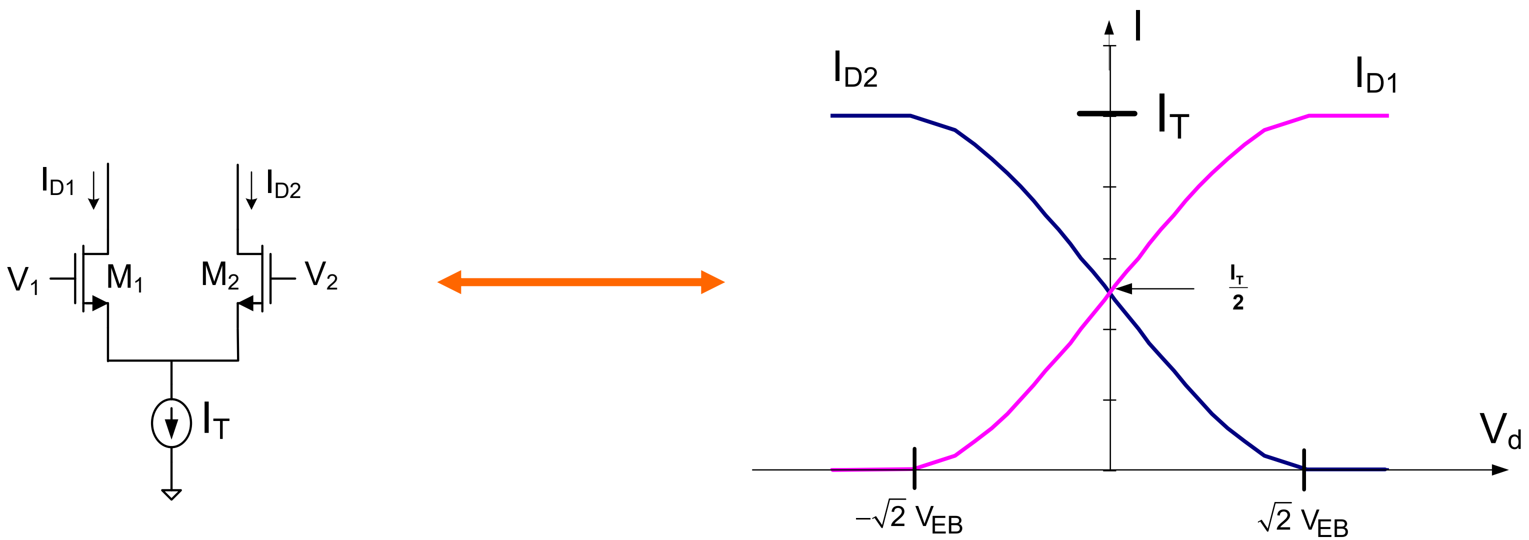
Current Steering DAC



Current Steering DAC

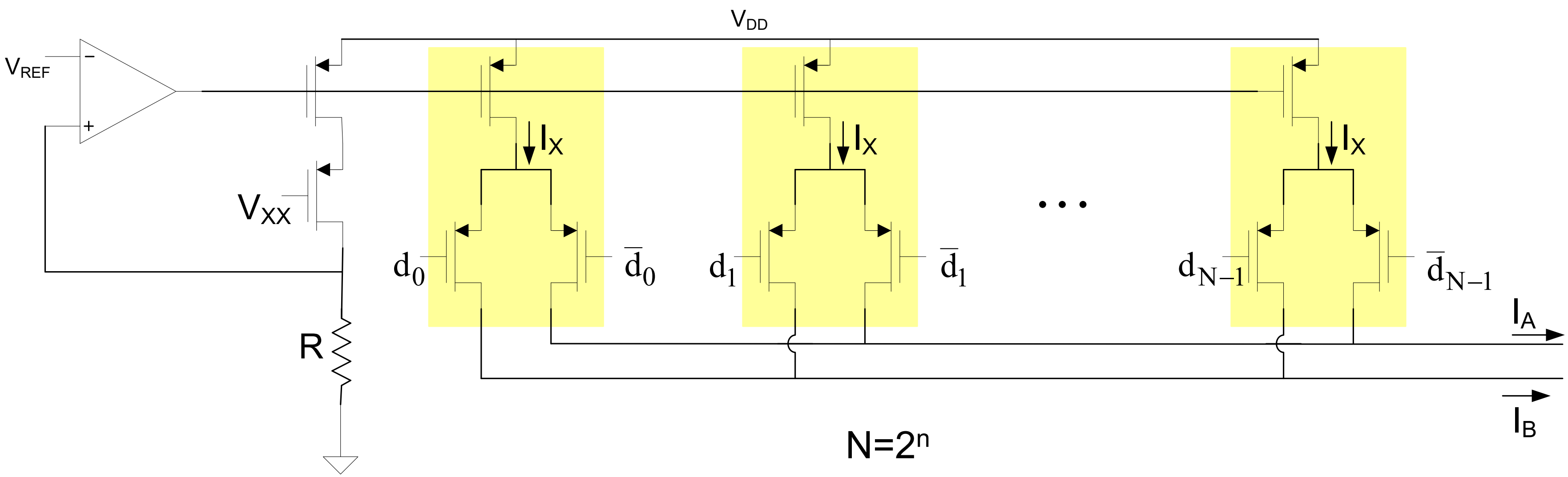






Review from Last Lecture

Current Steering DAC with Supply Independent Biasing



$N=2^n$

If transistors on top row are all matched, $I_X=V_{REF}/R$

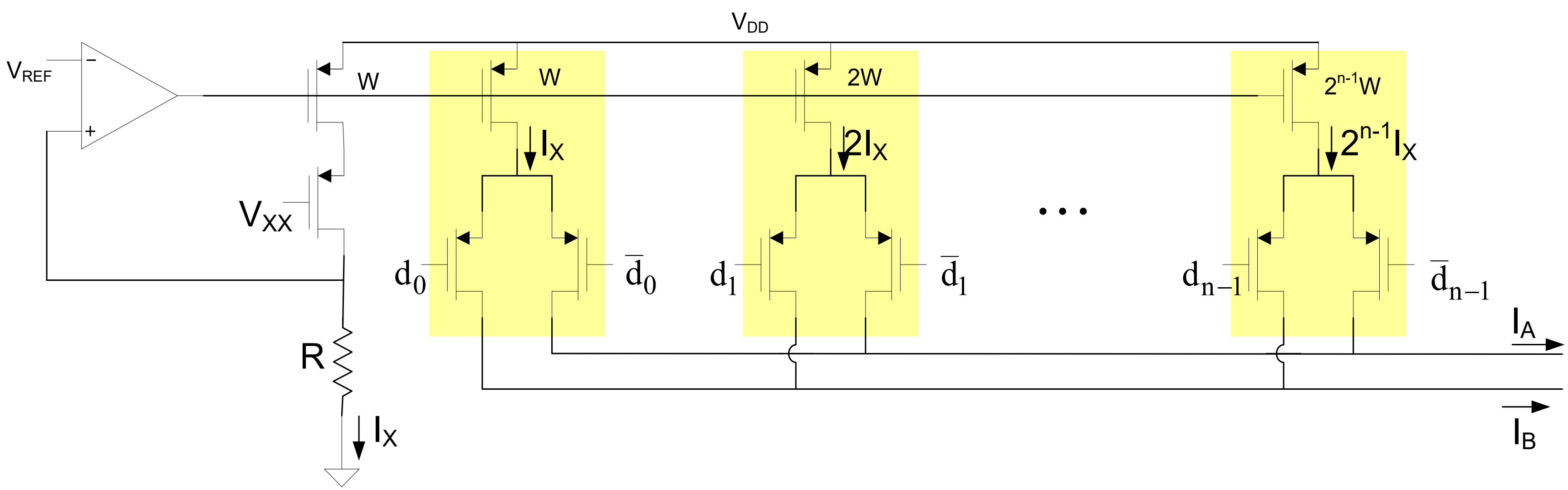
Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{N-1} d_i$$

Provides Differential Output Currents

Review from Last Lecture

Current Current Steering DAC with Supply Independent Biasing

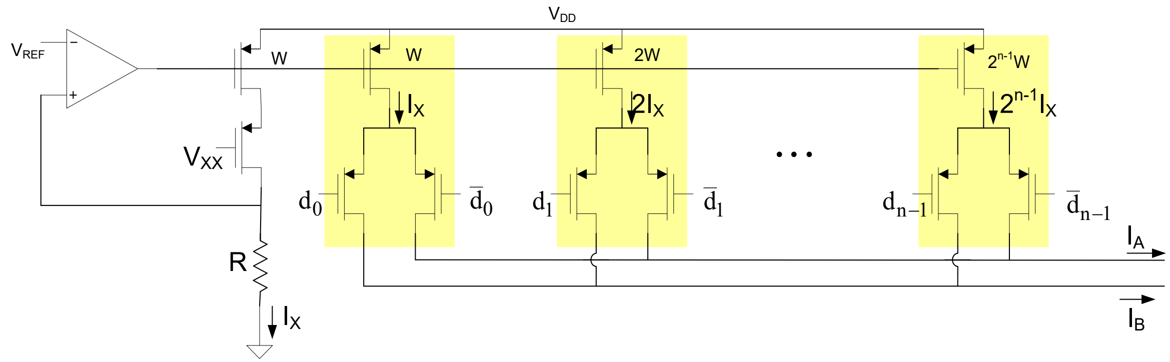


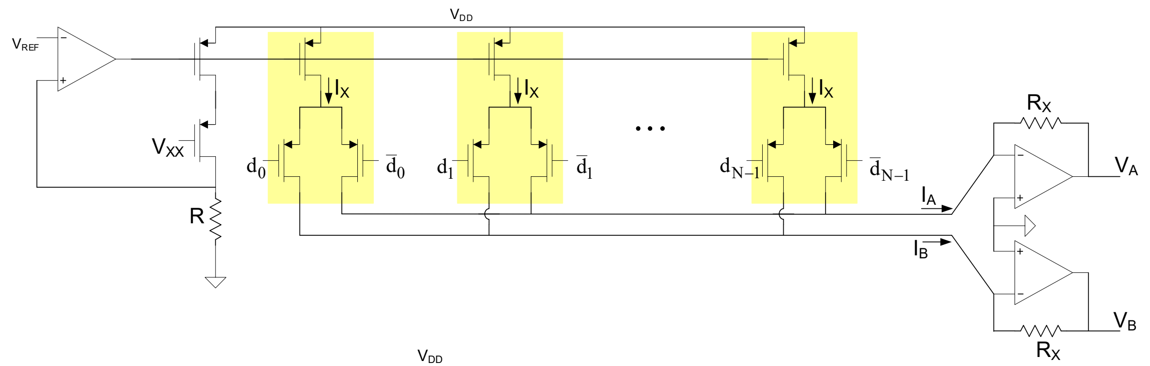
If transistors on top row are binary weighted

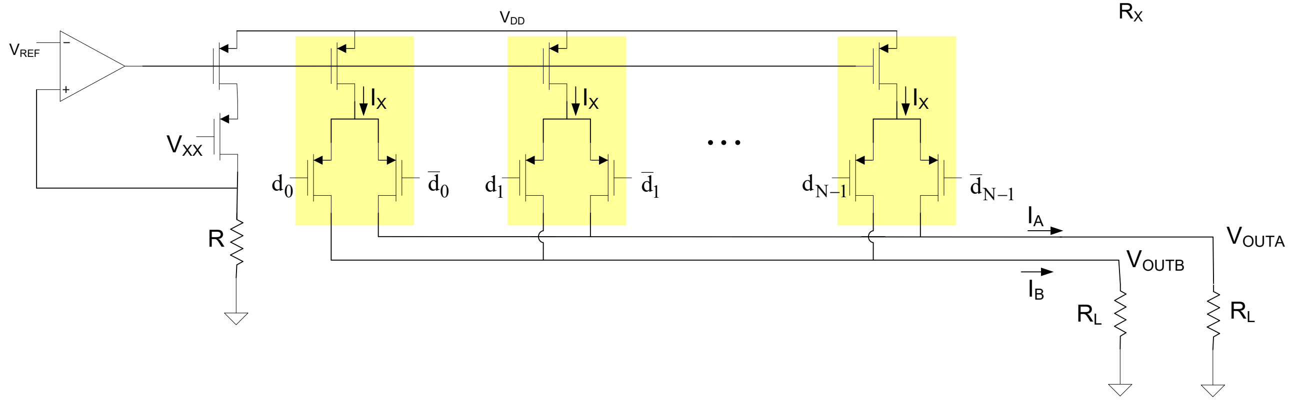
$$I_A = \left(\frac{V_{REF}}{R}\right)\sum_{i=0}^{n-1}\frac{d_i}{2^{n-i}}$$

Provides Differential Output Currents

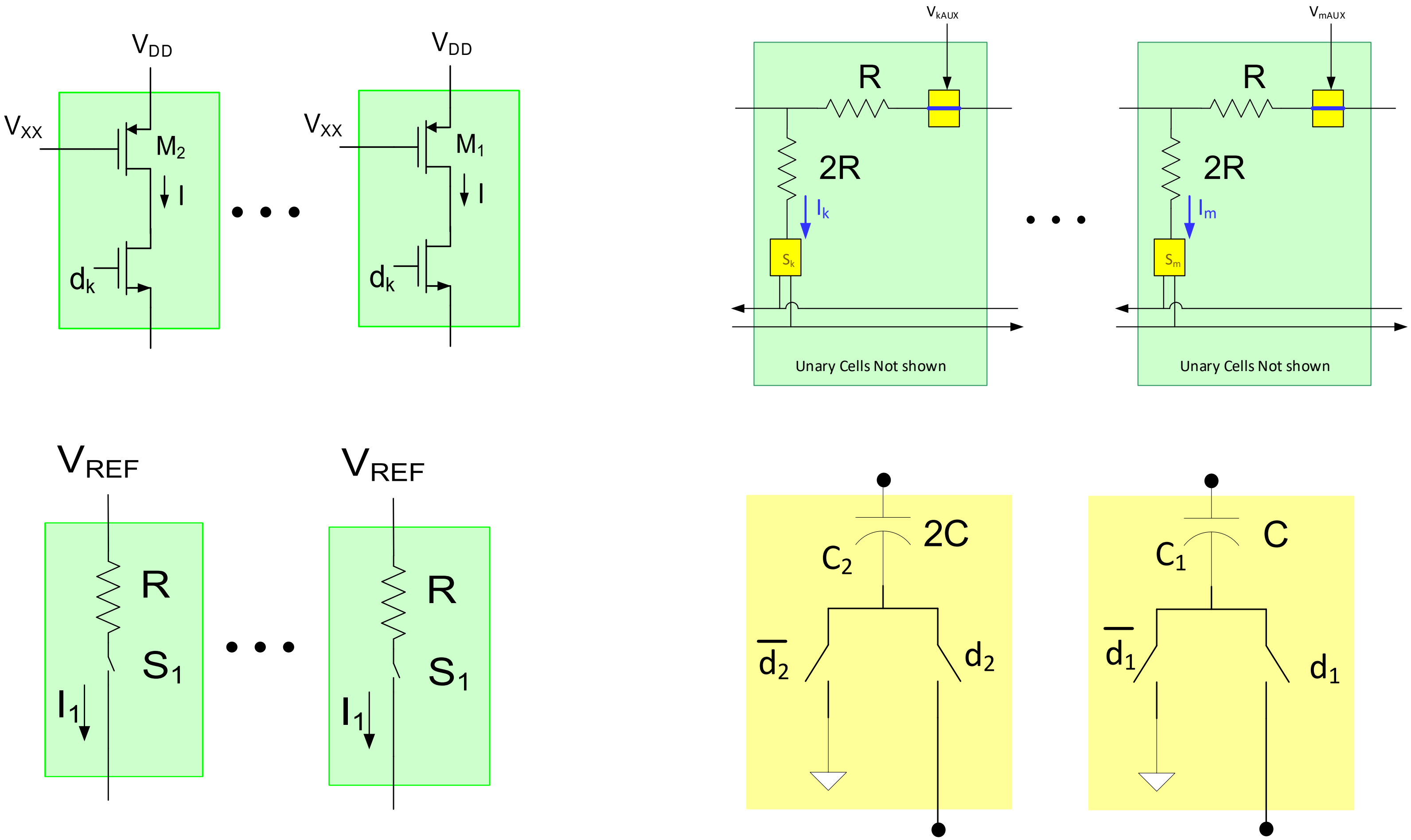
Current Steering DAC with current output, buffered output, resistor load





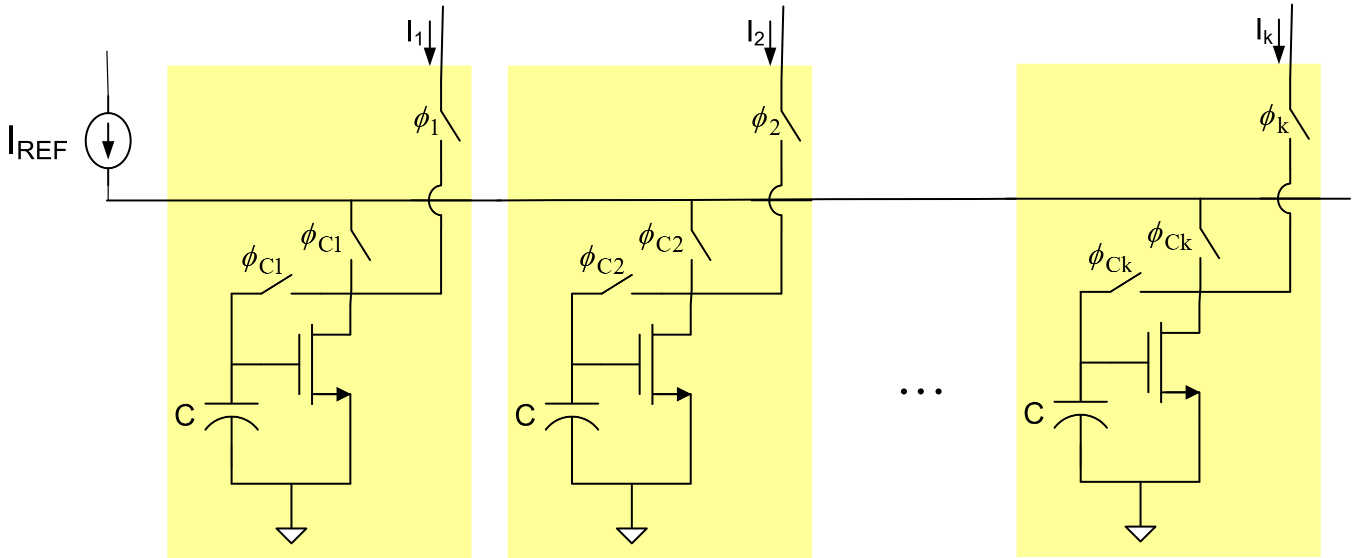


Matching is Critical in all DACs Considered



Obtaining adequate matching remains one of the major challenges facing the designer!

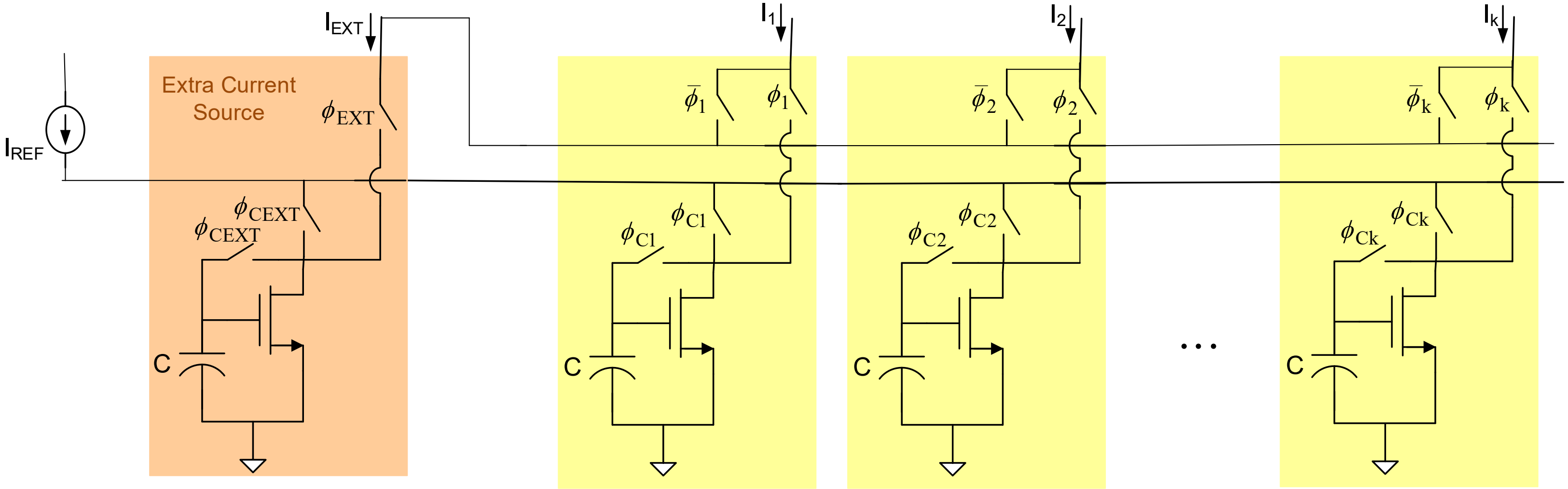
Dynamic Current Source Matching



- Correct charge is stored on C to make all currents equal to I_{REF}
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on C
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer or binary coded)
- Still use steering rather than switching in DAC

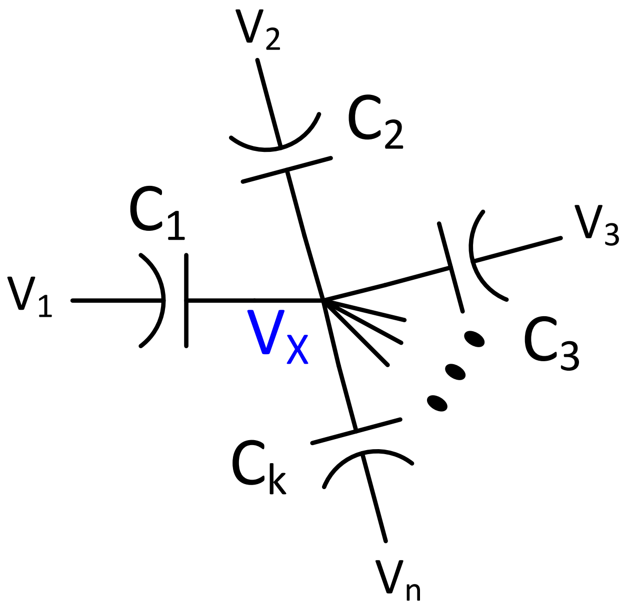
Often termed “Current Copier” or “Current Replication” circuit

Dynamic Current Source Matching



Extra current source can be added to facilitate background calibration

Charge Redistribution Principle



$$\sum_{i=1}^{k} C_i \left(V_k - V_X\right) = Q_X$$

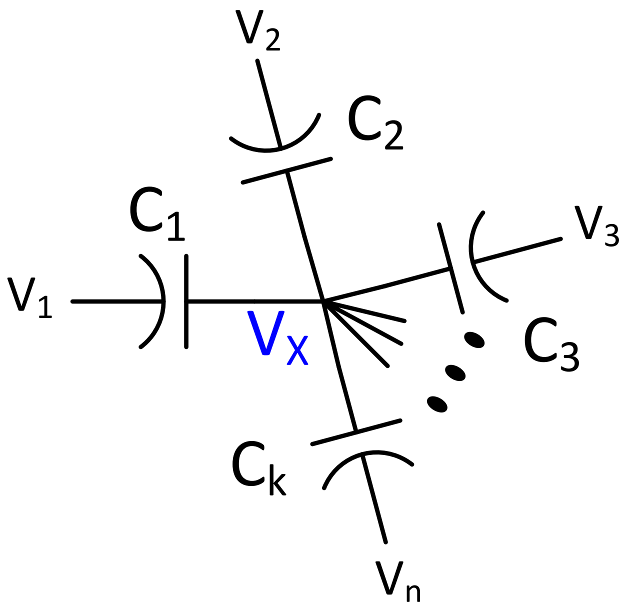
Charge on capacitors is preserved if there is no loss element on any of the capacitors

$$\sum_{i=1}^{k} C_i V_i - V_X \sum_{i=1}^{k} C_i = Q_X$$

Thus for any time-dependent voltages $V_1, \ldots V_k$

$$V_X = \frac{\sum_{i=1}^{k} C_i V_i - Q_X}{\sum_{i=1}^{k} C_i}$$

Charge Redistribution Principle

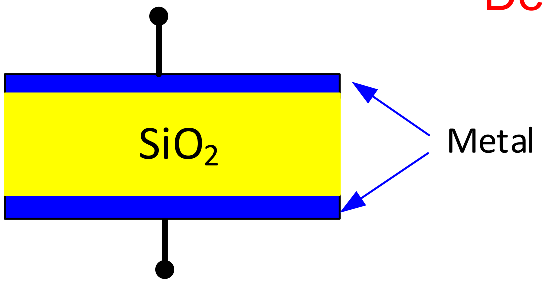


$$V_X = \frac{\sum_{i=1}^{k} C_i V_i - Q_X}{\sum_{i=1}^{k} C_i}$$

All capacitors will have some gradual leakage thus causing Q_T to change

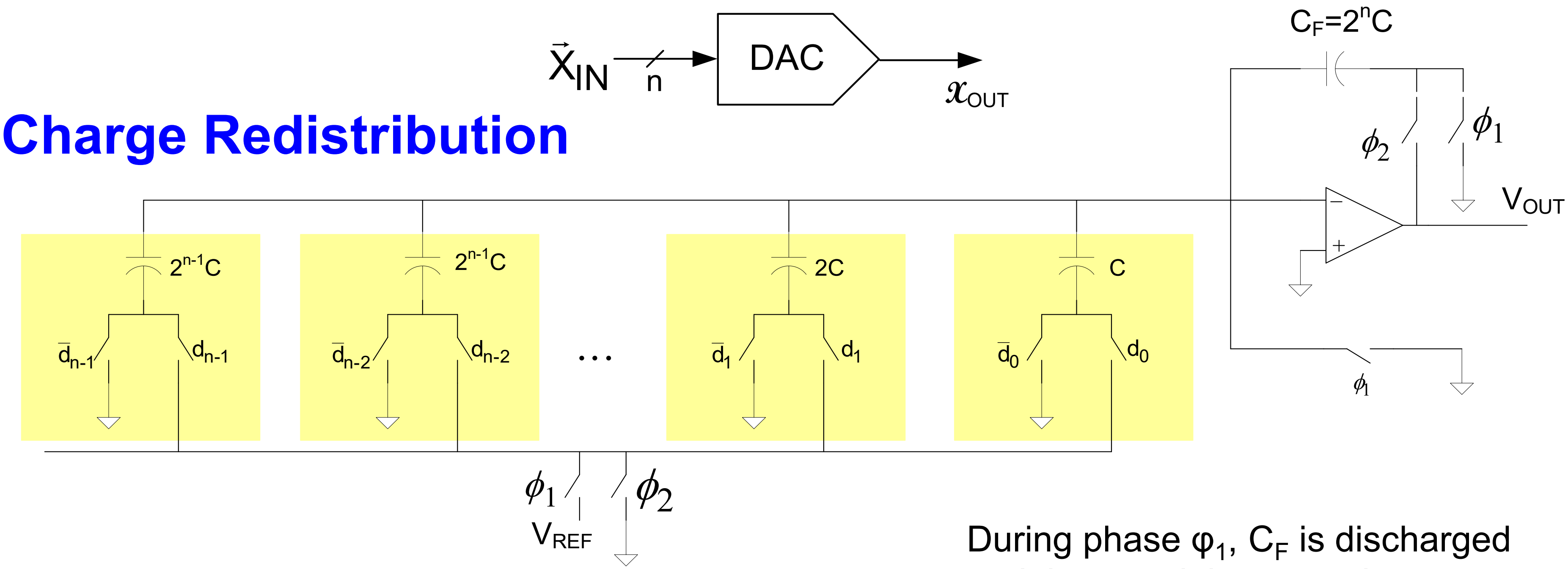
How long will charge on a simple M-SiO_2-M capacitor be retained in a standard semiconductor process?

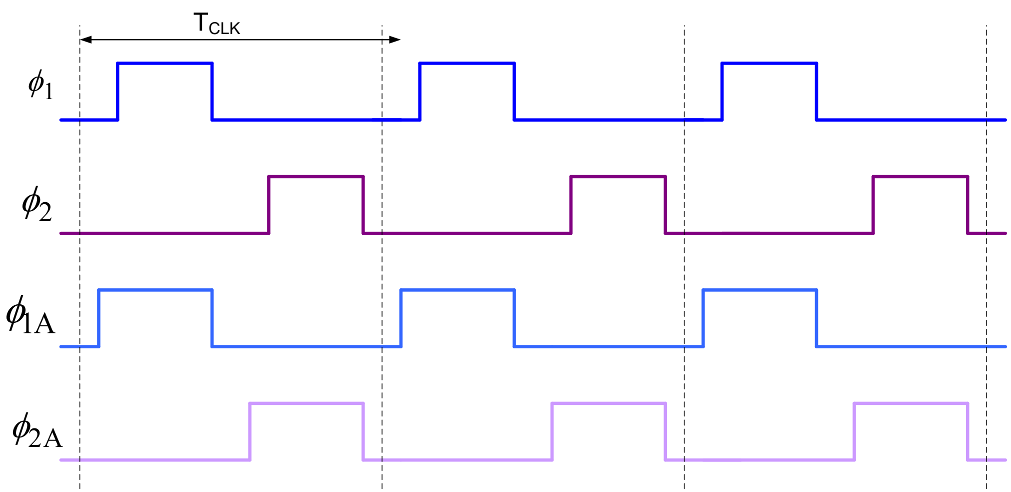
Decades !



DAC Architectures

Charge Redistribution





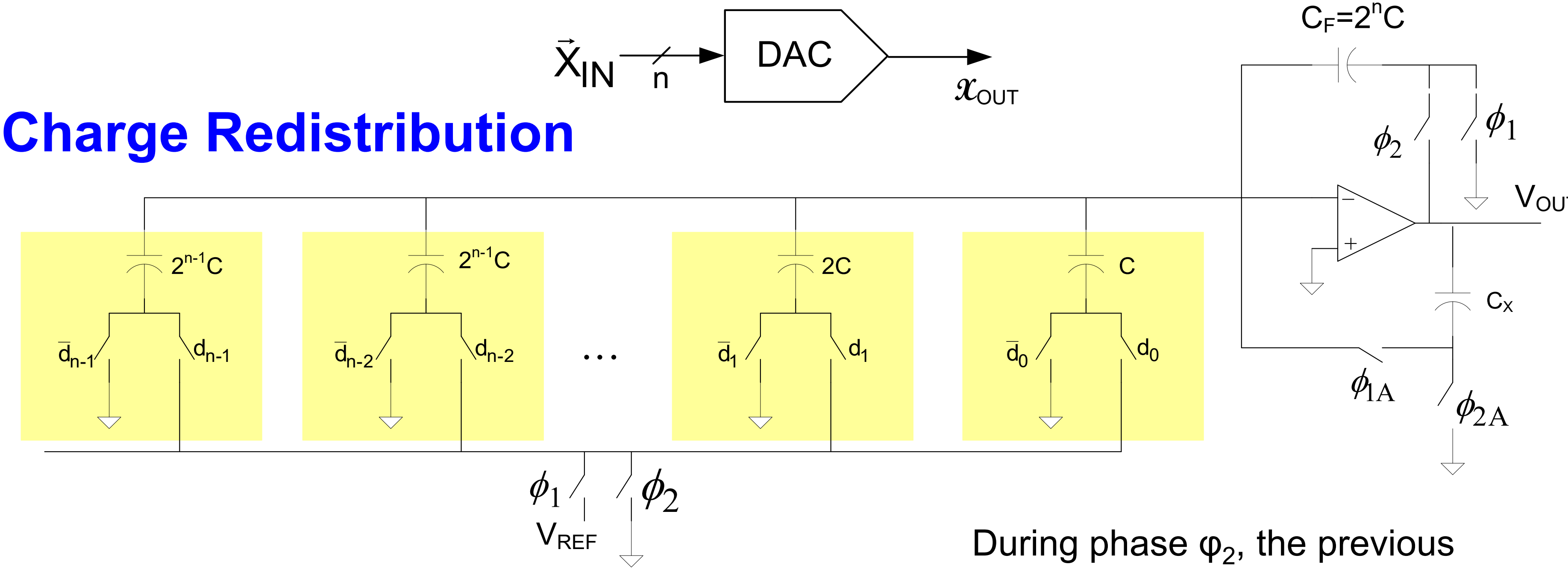
During phase φ_1, C_F is discharged and the remaining capacitors are charged to either V_{REF} or 0V depending upon Boolean input – total charge is denoted as Q_{SET}

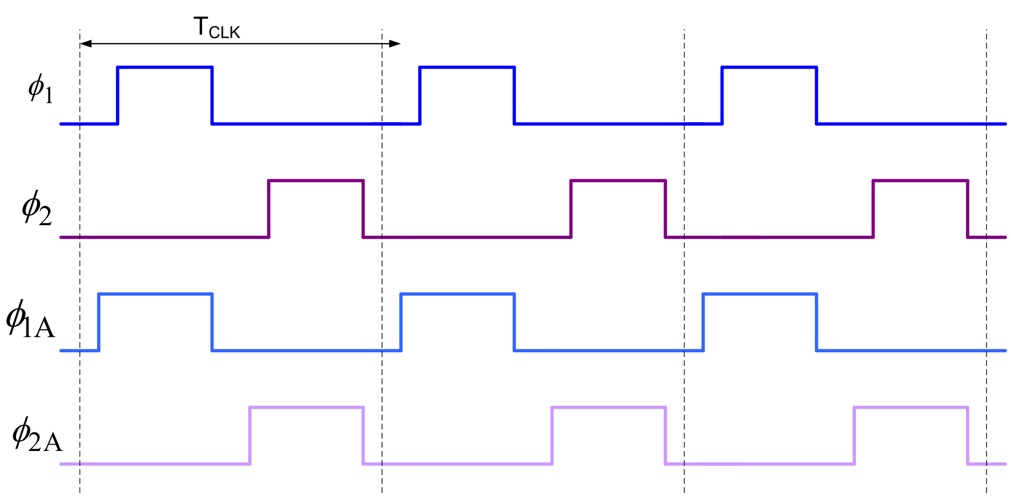
During phase φ_2, all charge on input-connected capacitors is transferred to C_F

DAC output voltage is $V_{OUT} = \frac{Q_{SET}}{C_F}$

DAC Architectures

Charge Redistribution



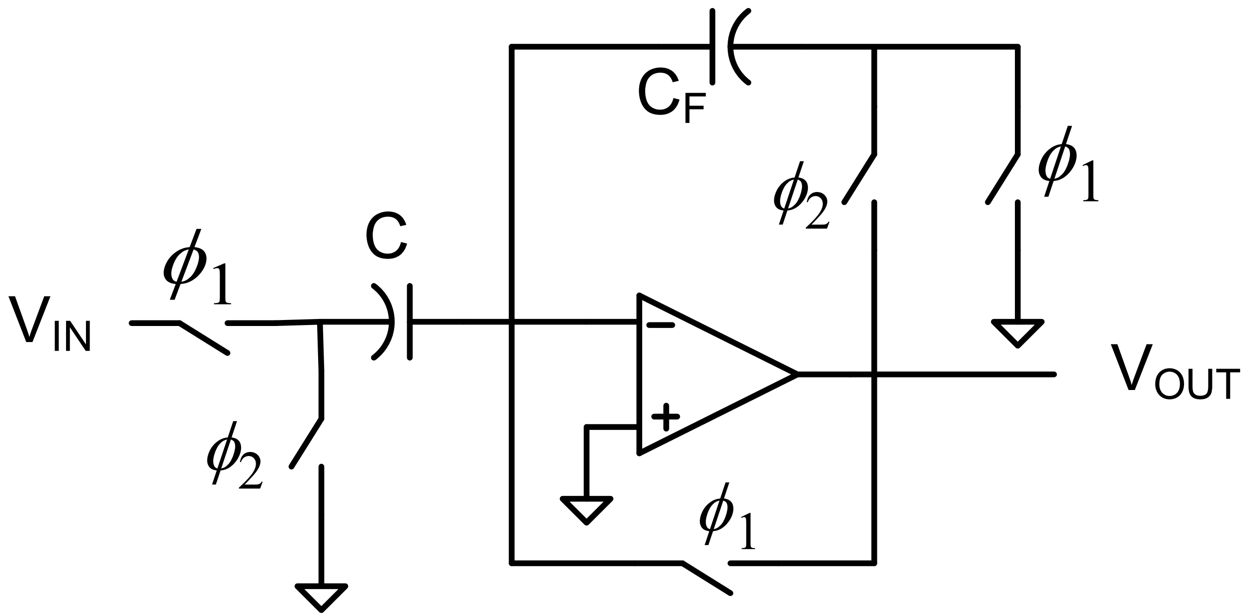


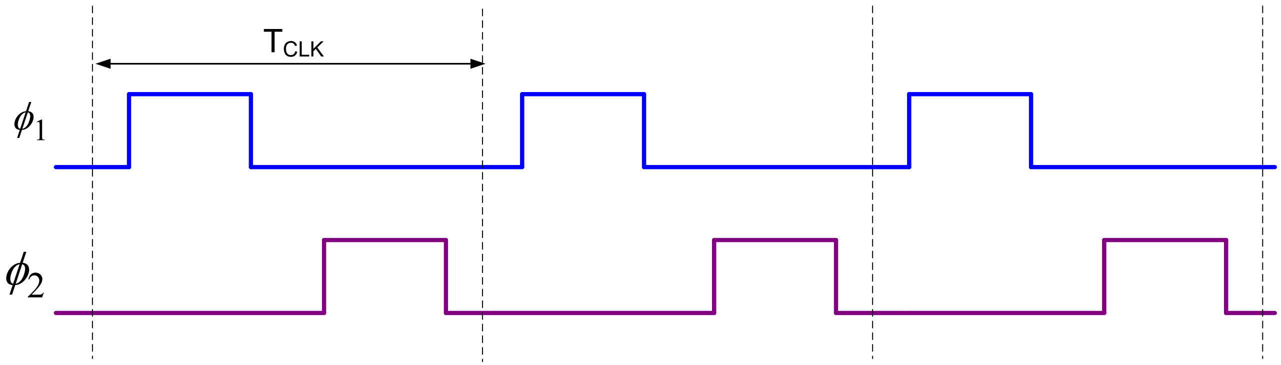
During phase φ_2, the previous output voltage is sampled on C_X

During phase φ_1, the Op Amp has feedback through C_X thus establishing a null-port at the input so voltage on selected sampling capacitors is V_{REF}

C_X does some good things
(mitigates V_{OS}, 1/f noise and finite gain errors)

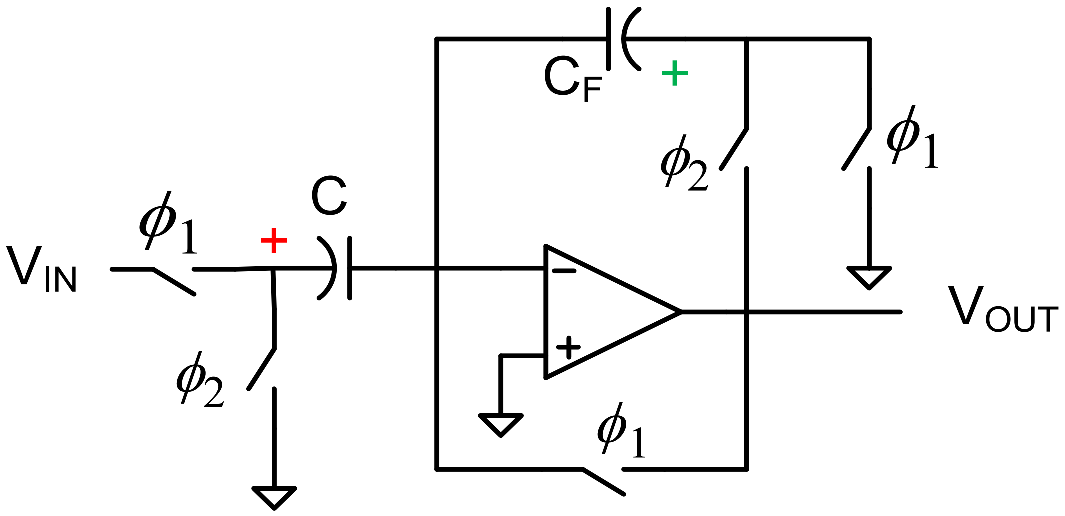
Consider basic charge redistribution circuit

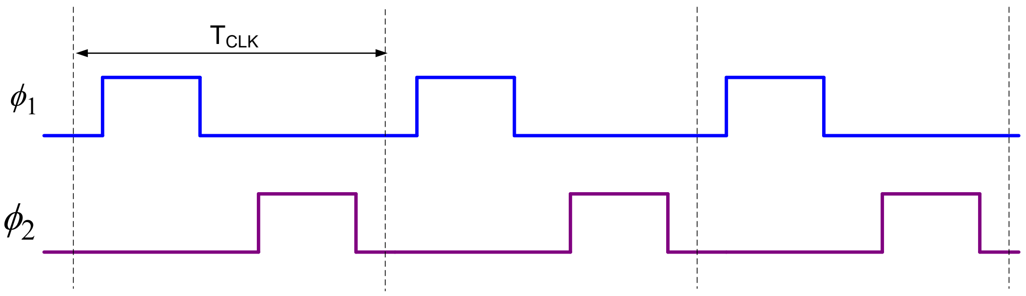




Clocks are complimentary non-overlapping

Basic charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

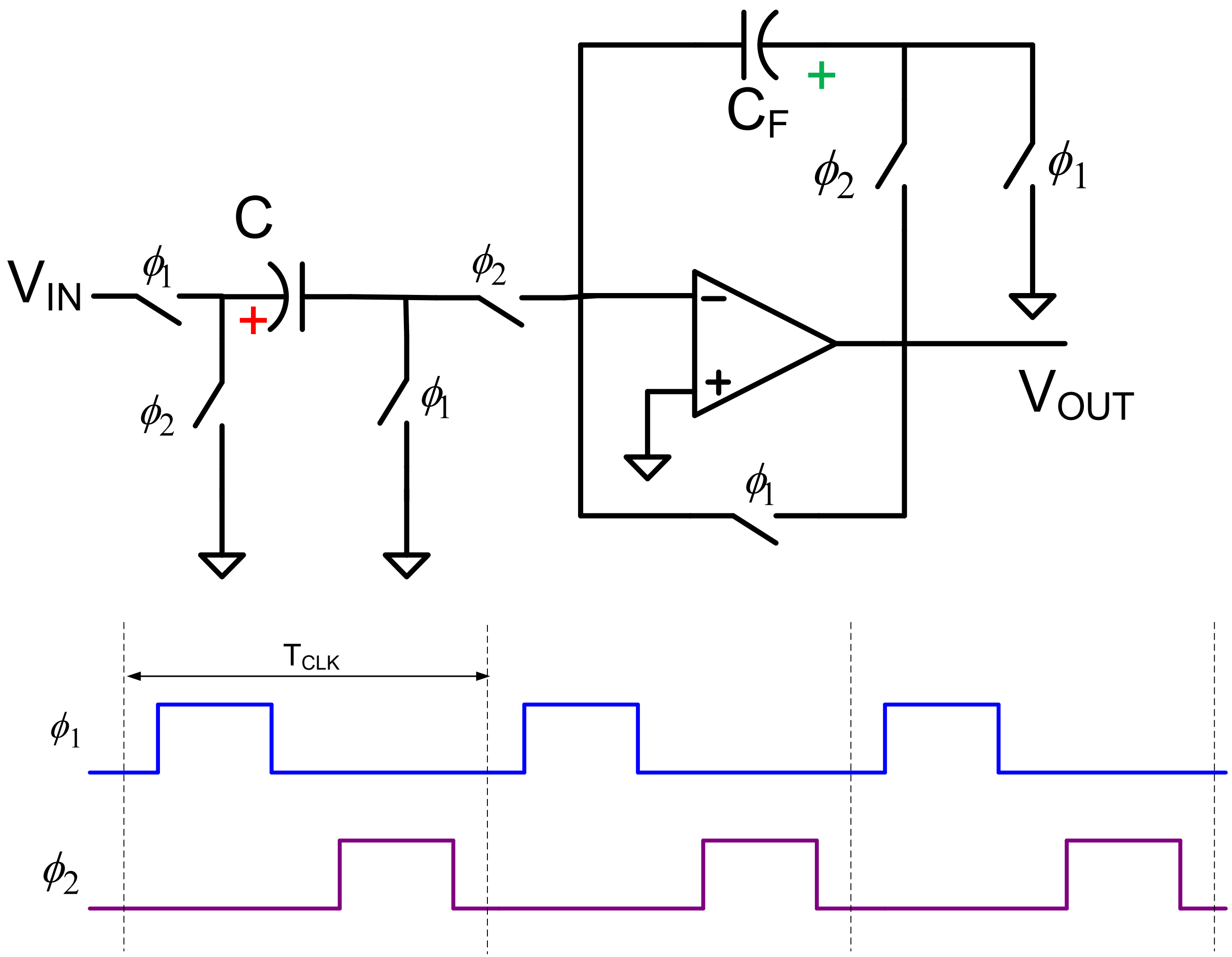
$$\frac{Q_{\phi 1}}{C_F} = V_{OUT}$$

$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

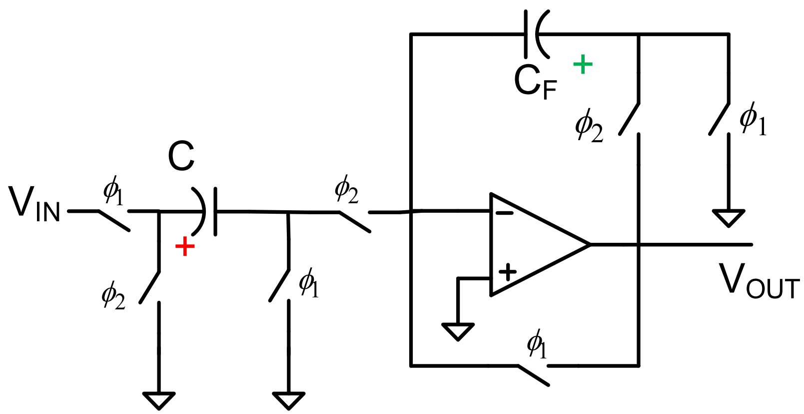
$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

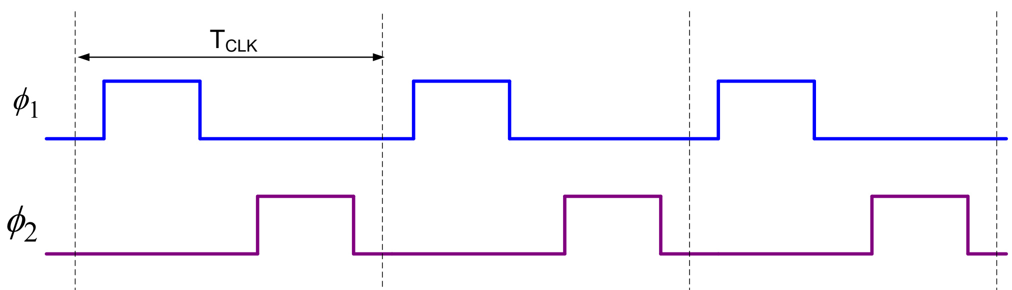
Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Another charge redistribution circuit



Another charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase φ_2

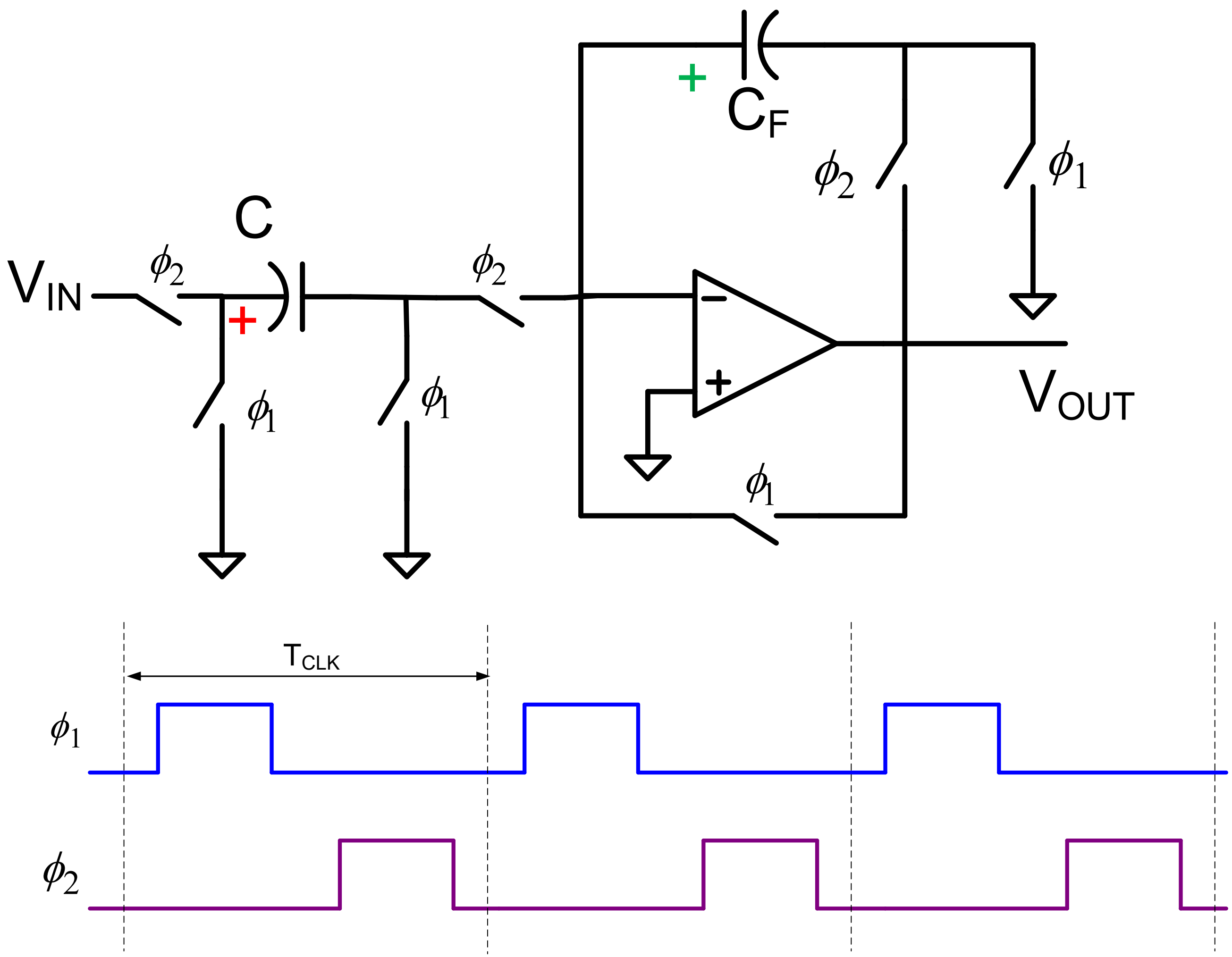
$$\frac{-Q_{\phi 1}}{C_F} = V_{OUT}$$

$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

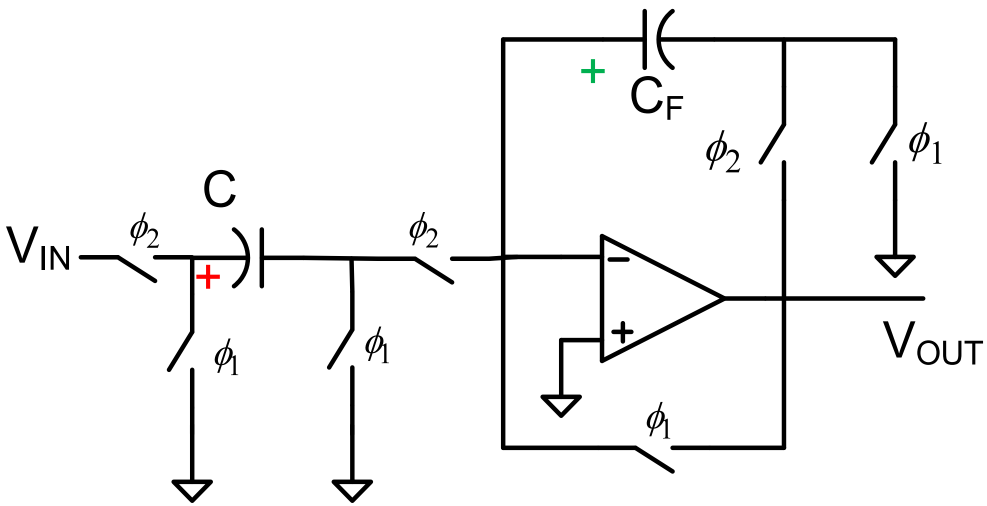
$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

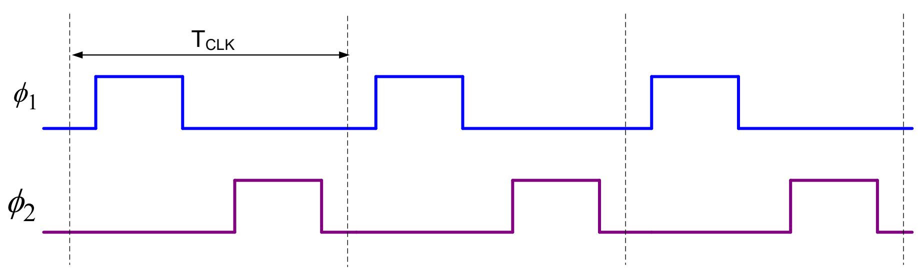
Serves as a noninverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Another charge redistribution circuit



Another charge redistribution circuit





During phase φ_1

$$Q_{\phi 1} = 0$$

$$Q_{CF} = 0$$

During phase φ_2

$$Q_{\phi 2} = CV_{IN}$$

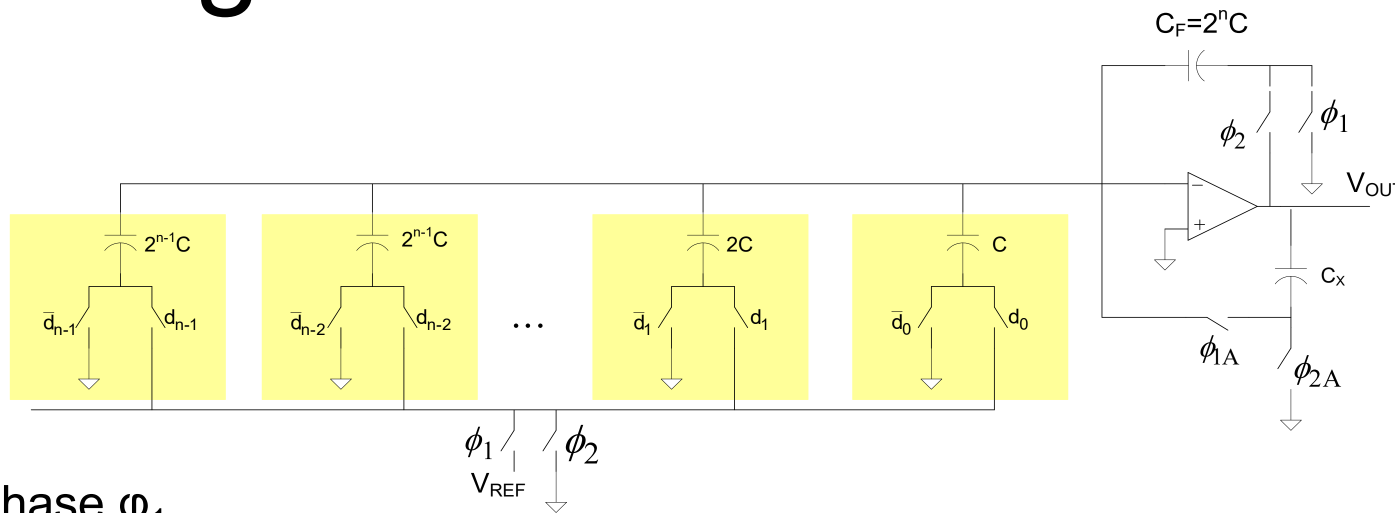
$$Q_{CF} = C_F V_{OUT}$$

$$Q_{CF} = -Q_{\phi 2}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as a inverting amplifier
Gain can be very accurate
Output valid only during Φ_2

Charge Redistribution DAC



During phase φ_1

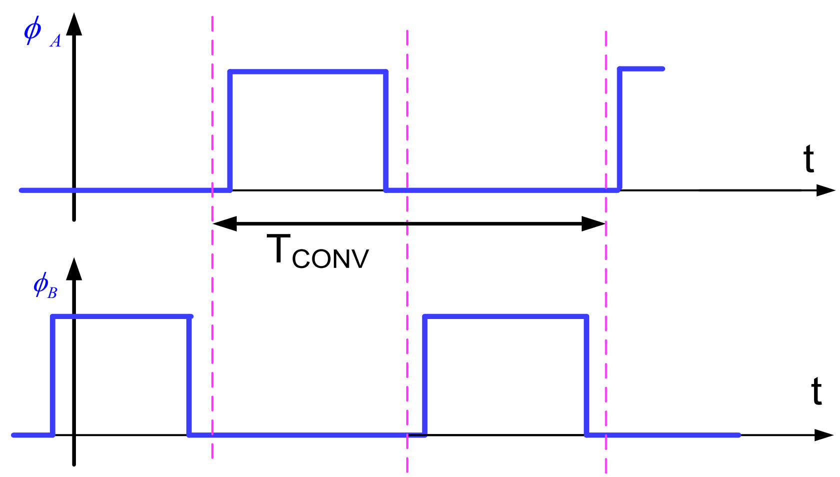
$$Q_{SET} = V_{REF} \sum_{i=0}^{n-1} d_i 2^i C$$

During phase φ_2

Charge Q_{SET} is all transferred to C_F

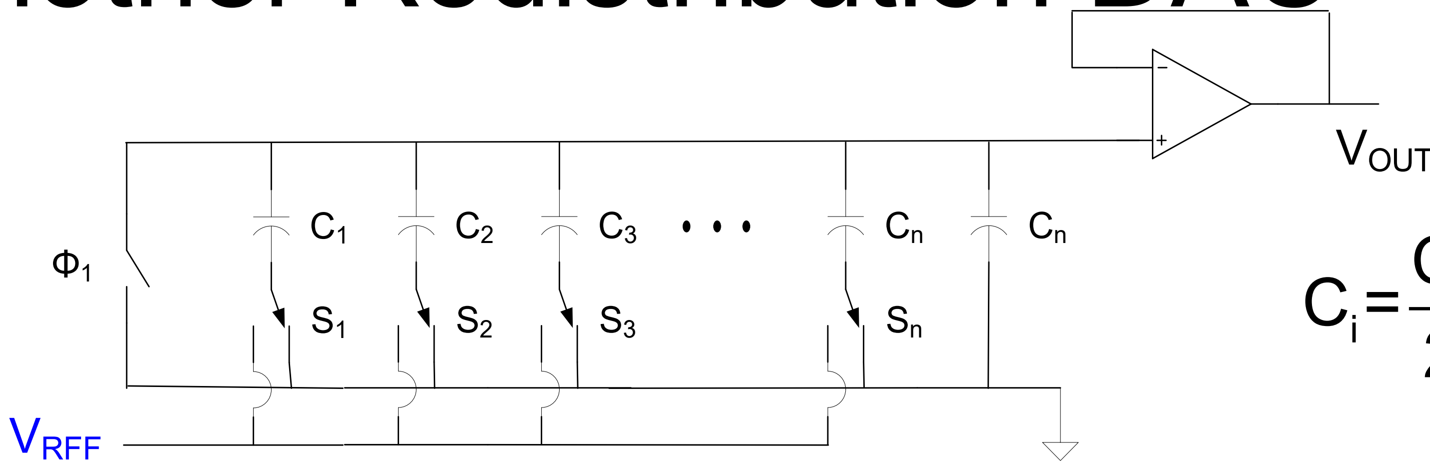
$$Q_{CF} = V_{OUT} 2^n C$$

but $$Q_{SET} = Q_{CF}$$



$$V_{REF} \sum_{i=0}^{n-1} d_i 2^i C = V_{OUT} 2^n C \quad \Rightarrow \quad V_{OUT} = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Another Redistribution DAC



$$C_i = \frac{C}{2^i}$$

During phase φ_1 selected switches set to V_{REF}

$$Q_{SET} = V_{REF}\sum_{i=0}^{n} d_i C_i = V_{REF}\sum_{i=0}^{n} d_i \frac{C}{2^{n-i}}$$

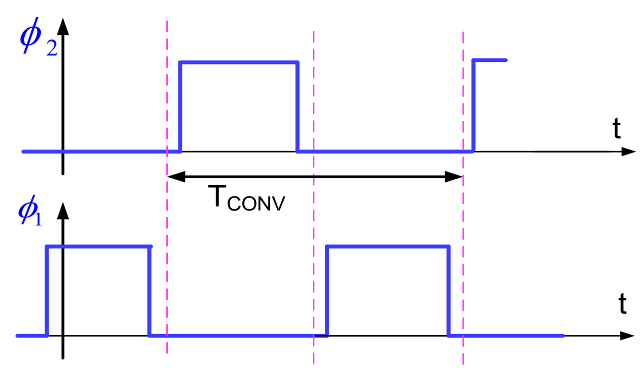
During phase φ_2 all switches connected to GND

Charge Q_{SET} is all redistributed among the capacitors

$$Q_{SET} = V_{OUT}\left(\sum_{i=1}^{n} C_i + C_n\right)$$

but

$$\sum_{i=1}^{n} C_i + C_n = \left(\sum_{i=1}^{n} \frac{C}{2^i} + C_n\right) = C$$

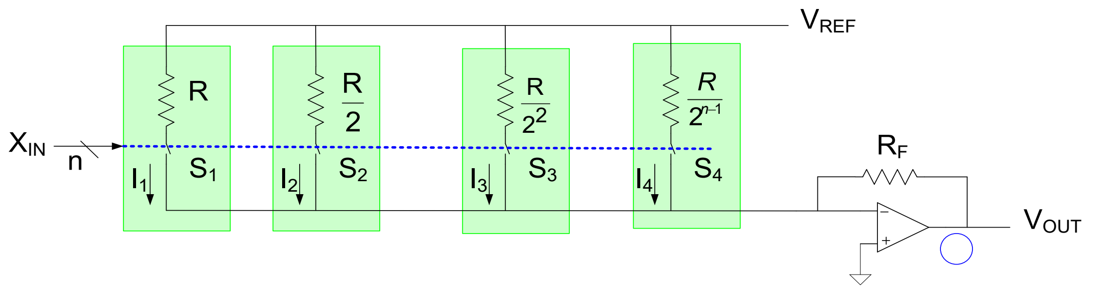


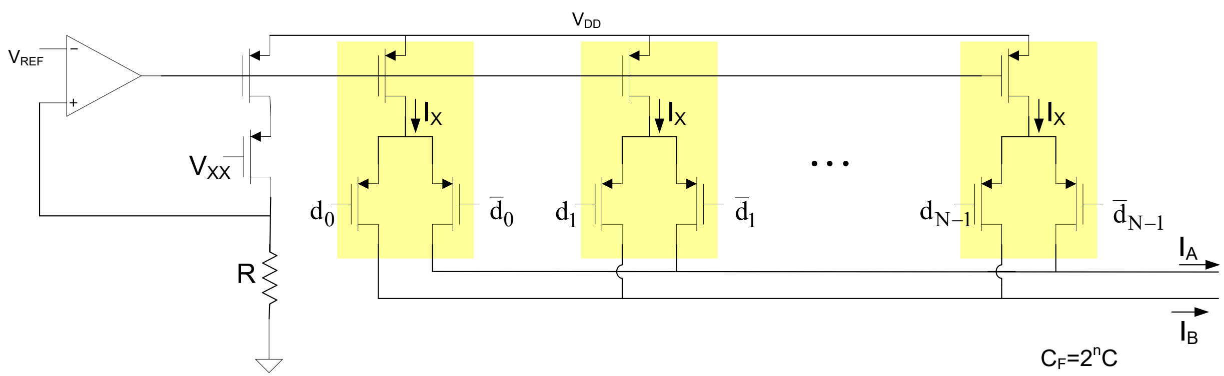
$$Q_{SET} = V_{OUT} C$$

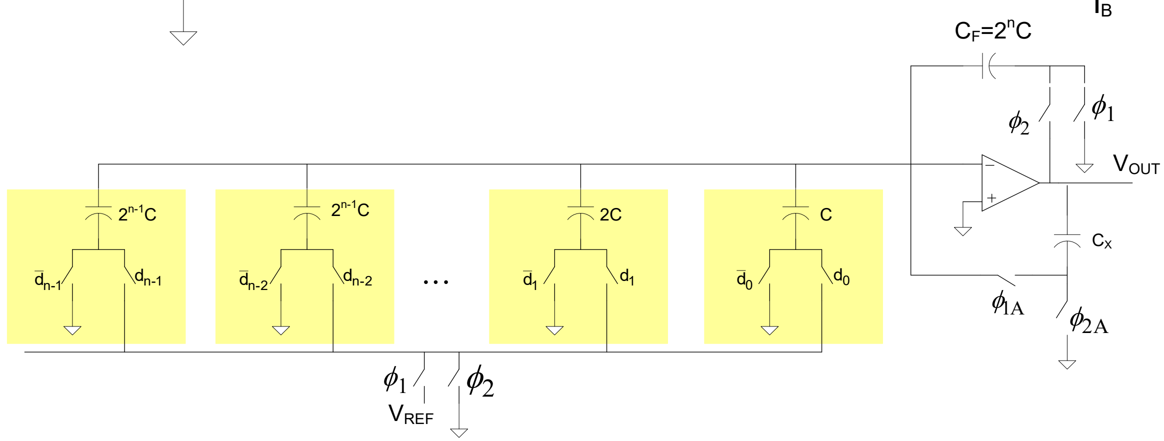
$$V_{REF}\sum_{i=0}^{n-1} d_i \frac{C}{2^{n-i}} = V_{OUT} C \quad \Rightarrow \quad V_{OUT} = V_{REF}\sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?



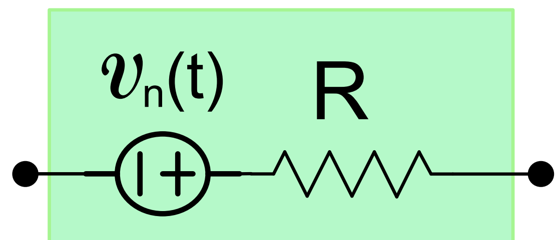




Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in resistors:



Noise spectral density of $v_n(t)$ at all frequencies $S = 4kTR$

This is white noise !

k: Boltzmann's Constant
T: Temperature in Kelvin

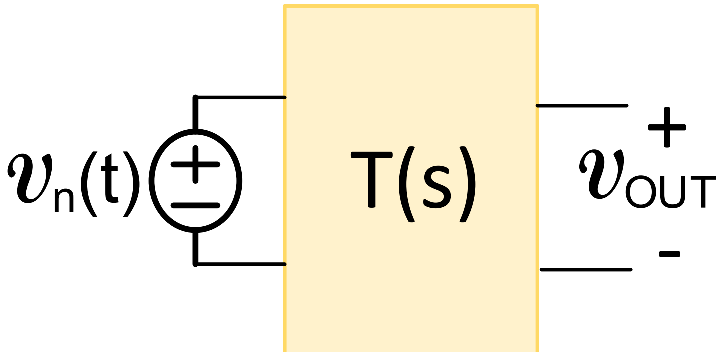
$k=1.38064852 \times 10^{-23}\ m^2\ kg\ s^{-2}\ K^{-1}$

At 300K, $kT=4.14 \times 10^{-21}$

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in linear circuits:

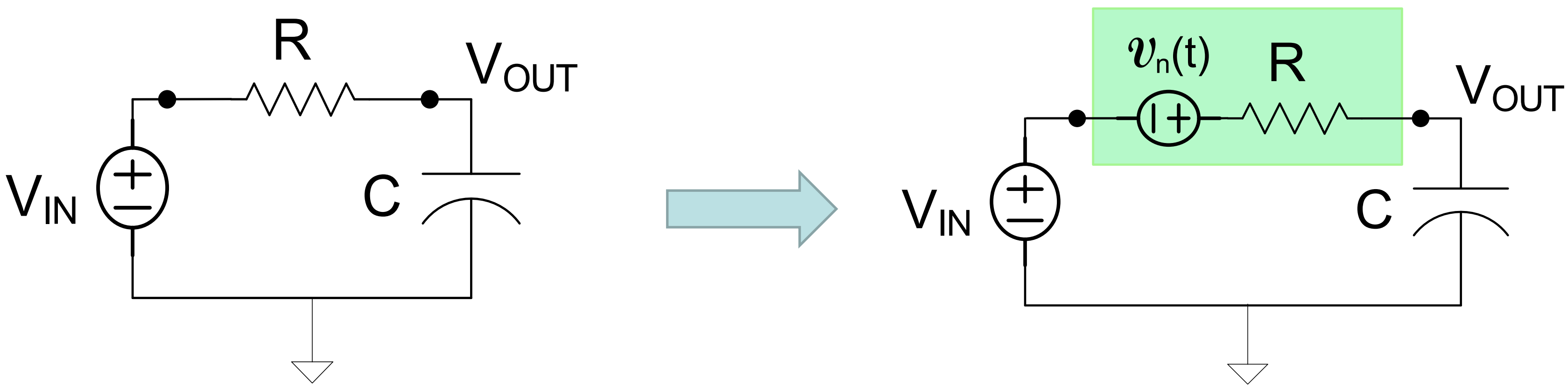


Due to any noise voltage source:

$$S_{V_{OUT}} = S_{V_n} \left|T(j\omega)\right|^2$$

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left|T(j\omega)\right|^2 df}$$

Example: First-Order RC Network

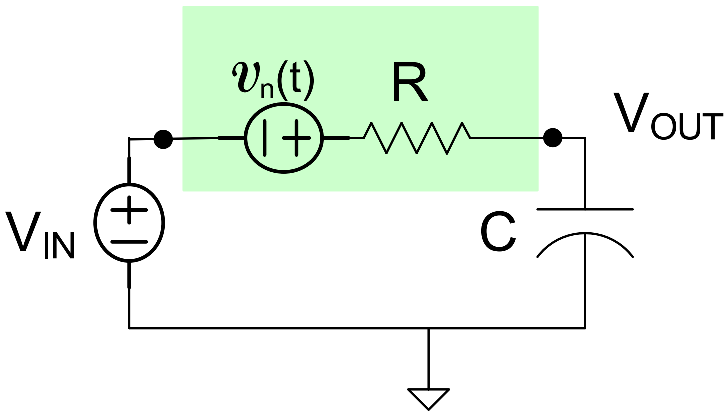


$$T(s) = \frac{1}{1+RCs}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\, df}$$

Example: First-Order RC Network

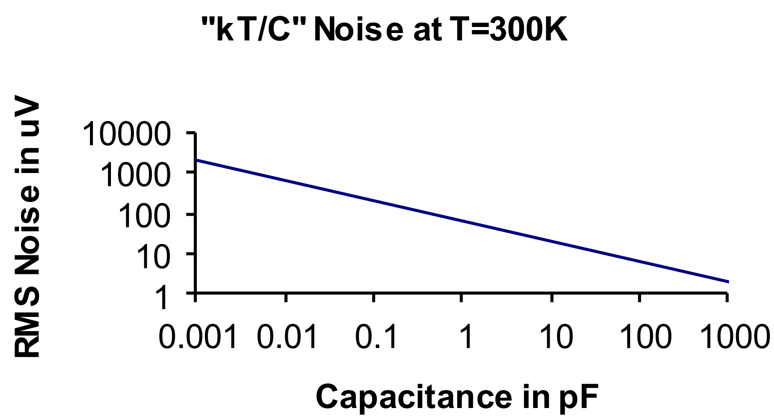


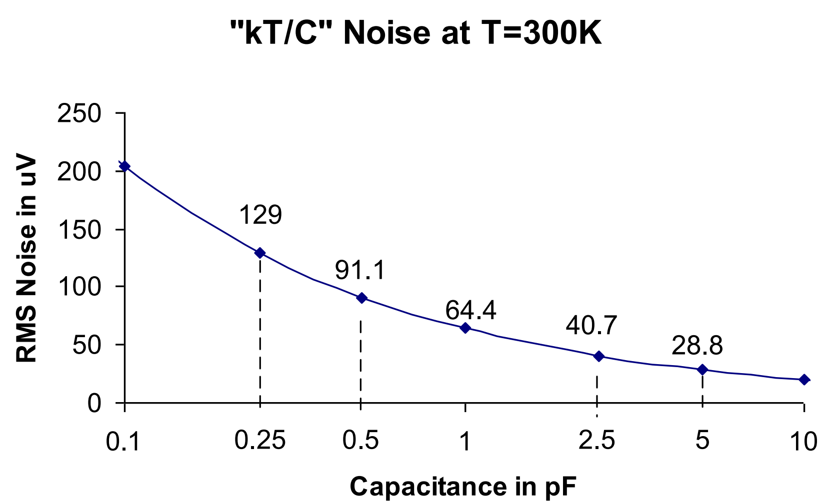
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2 R^2 C^2}\, df}$$

From a standard change of variable with a trig identity, it follows that

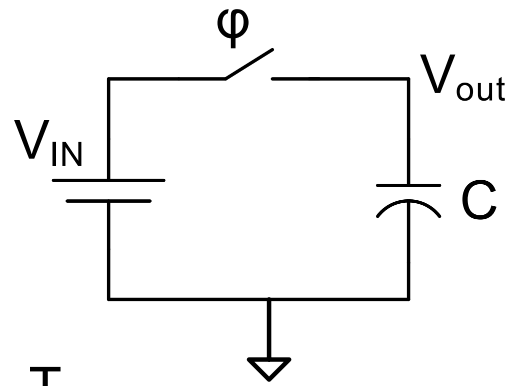
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$

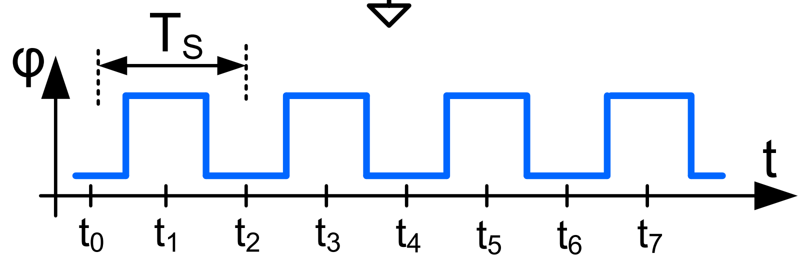
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C

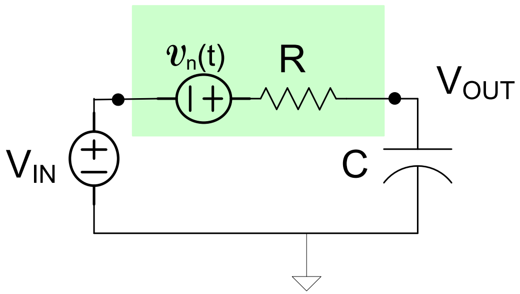

"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF


"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

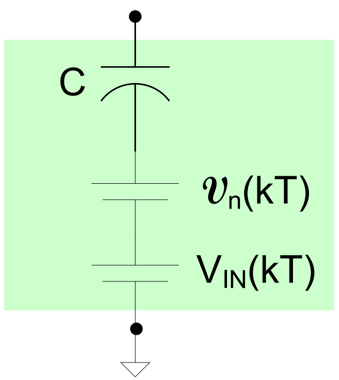
Example: Switched Capacitor Sampler





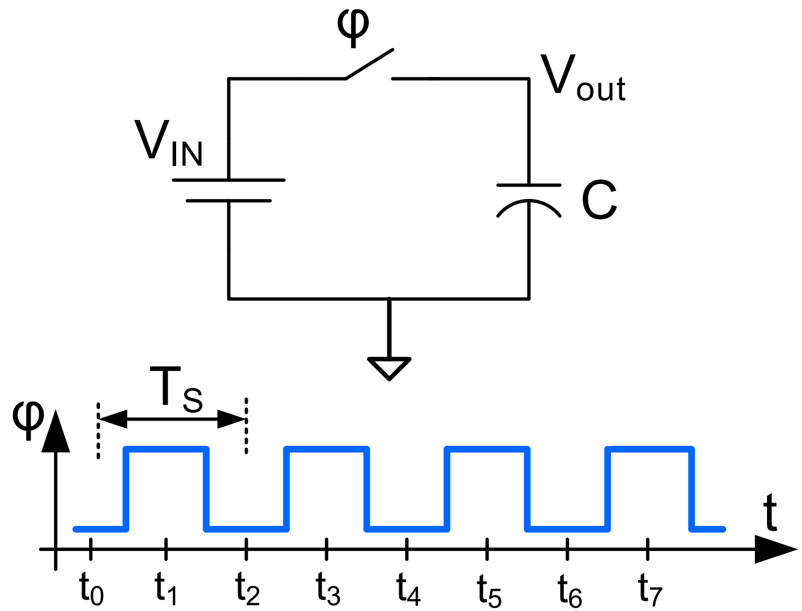


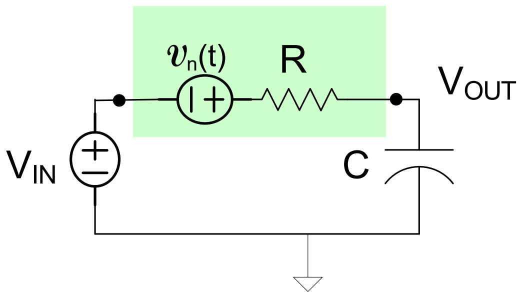
Track mode



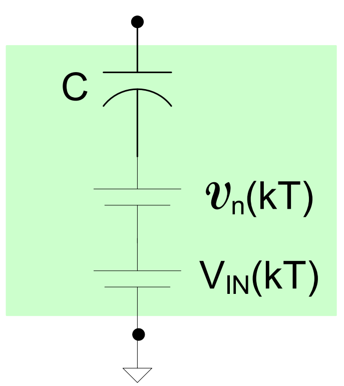
Hold mode

Example: Switched Capacitor Sampler





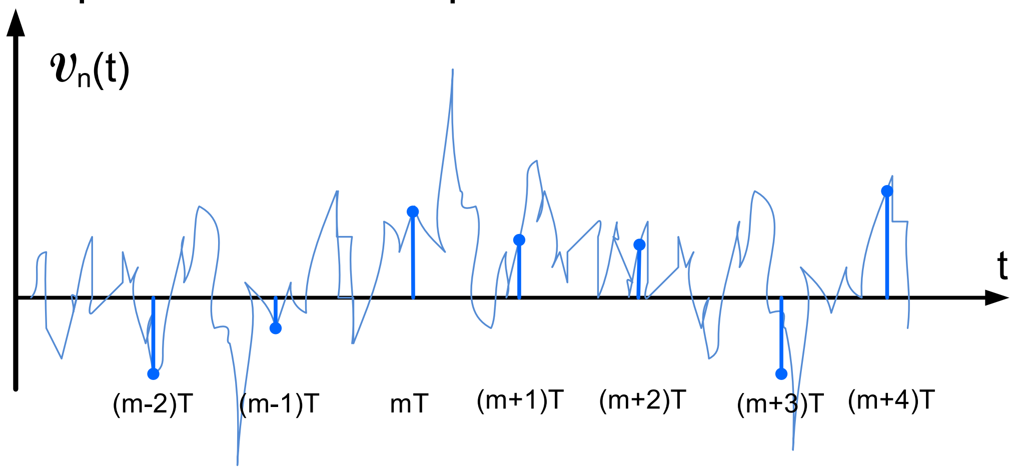
Track mode

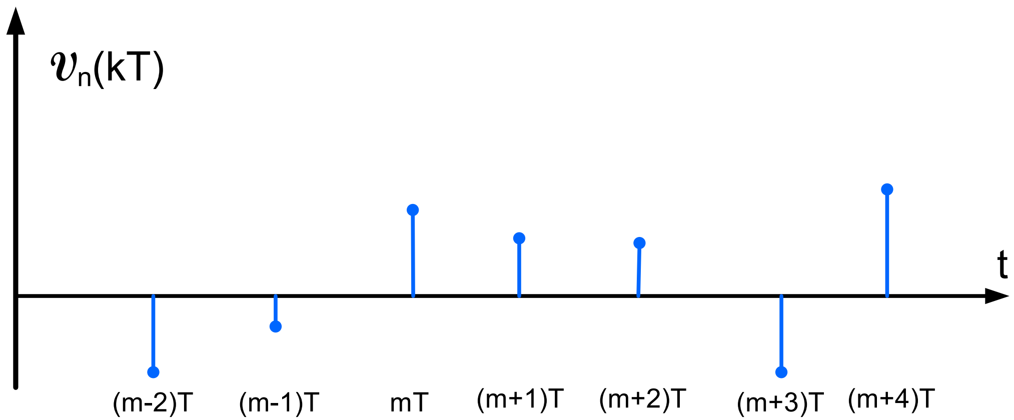


Hold mode

Example: Switched Capacitor Sampler

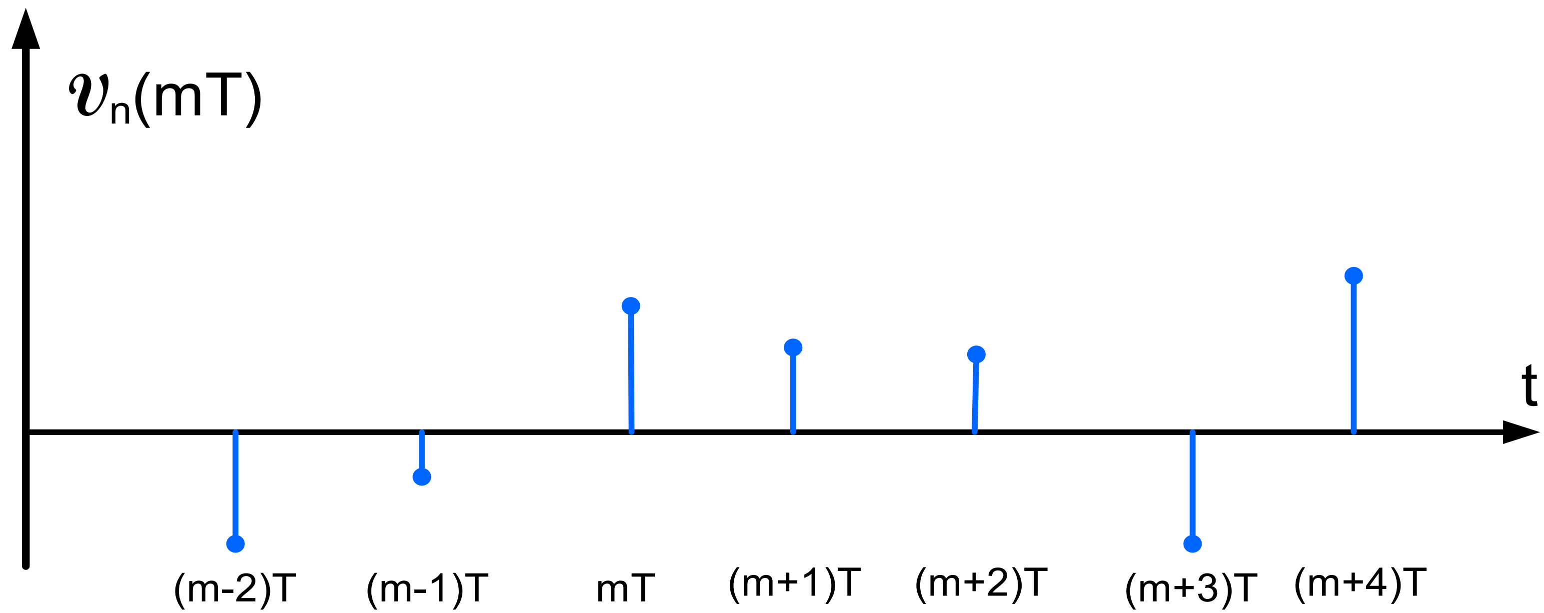
T is the period of the sampler





$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

Characterization of a noise sequence

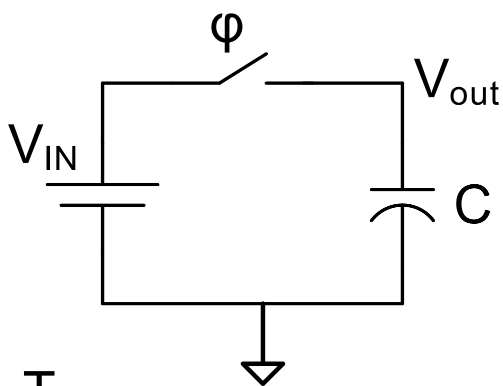


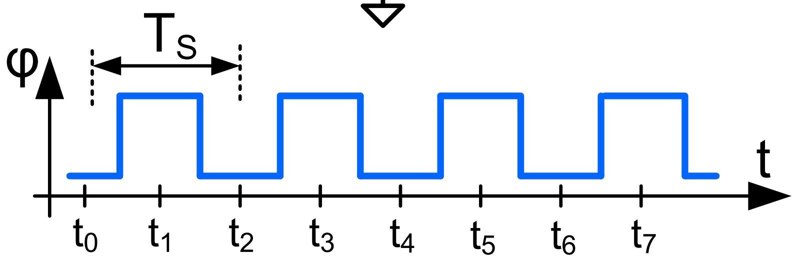
$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\,large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

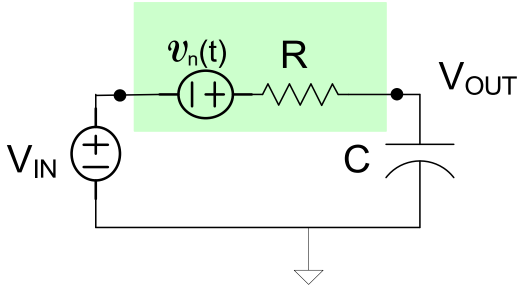
Theorem If $\mathcal{V}(t)$ is a continuous-time zero-mean noise source and <$\mathcal{V}(kT)$> is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $\mathcal{V}_{\text{RMS}} = \hat{\mathcal{V}}_{\text{RMS}}$

Theorem If $\mathcal{V}(t)$ is a continuous-time zero-mean noise signal and <$\mathcal{V}(kT)$> is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $\mathcal{V}(kT)$, denoted as $\sigma_{\hat{V}}$ satisfies the expression $\sigma_{\hat{V}} = \mathcal{V}_{\text{RMS}} = \hat{\mathcal{V}}_{\text{RMS}}$

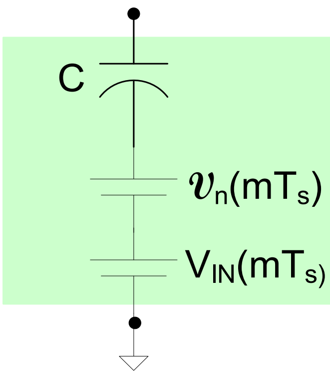
Example: Switched Capacitor Sampler







Track mode



Hold mode

$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

k: Boltzmann's constant

T: temperature in Kelvin

End of Lecture 18